

ABSTRACT OF THE DISCLOSURE

The present invention relates in general to integrated circuits, and in particular to method and circuitry for implementing an improved phase-locked loop (PLL) in complementary metal-oxide-semiconductor (CMOS) technology using current-controlled CMOS (C³MOS) logic. In an exemplary embodiment, a phase-locked loop includes a phase-frequency detector, a Gm cell block, a low pass filter and a voltage controlled oscillator. These various elements of the phase-locked loop are connected to one another in a fully differential manner, i.e., each element has an input and/or an output each having at least a differential signal. In one embodiment, each of these various elements of the phase-locked loop is implemented using C³MOS logic.

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